MINIMIZATION OF THE LOCAL RESIDUAL STRESS IN 3D FLIP CHIP STRUCTURES BY OPTIMIZING THE MECHANICAL PROPERTIES OF ELECTROPLATED MATERIALS AND THE ALIGNMENT STRUCTURE OF TSVS AND FINE BUMPS

Kohta Nakahira
Tohoku University
Sendai, Miyagi, Japan

Hironori Tago
Tohoku University
Sendai, Miyagi, Japan

Fumiaki Endo
Tohoku University
Sendai, Miyagi, Japan

Ken Suzuki
Tohoku University
Sendai, Miyagi, Japan

Hideo Miura
Tohoku University
Sendai, Miyagi, Japan

ABSTRACT
Since the thickness of the stacked silicon chips in 3D integration has been thinned to less than 100 μm, the local thermal deformation of the chips has increased drastically because of the decrease of the flexural rigidity of the thinned chips. The clear periodic thermal deformation and thus, the thermal residual stress distribution appears in the stacked chips due to the periodic alignment of metallic bumps, and they deteriorate the reliability of products. In this paper, the dominant structural factors of the local residual stress in a silicon chip are discussed quantitatively based on the results of a three-dimensional finite element analysis and the measurement of the local residual stress in a chip using stress sensor chips. The piezoresistive strain gauges were embedded in the sensor chips. The length of each gauge was 2 μm, and an unit cell consisted of 4 gauges with different crystallographic directions. This alignment of strain gauges enables to measure the tensor component of three-dimensional stress fields separately. Test flip chip substrates were made by silicon chip on which the area-arrayed tin/copper bumps were electroplated. The width of a bump was fixed at 200 μm, and the bump pitch was varied from 400 μm to 1000 μm. The thickness of the copper layer was about 40 μm and that of tin layer was about 10 μm. This tin layer was used for the rigid joint formation by alloying with copper interconnection formed on a stress sensing chip. The measured amplitude of the residual stress increased from about 30 MPa to 250 MPa depending on the combination of materials such as bump, underfill, and interconnections. It was confirmed that both the material constant of underfill and the alignment structure of fine bumps are the dominant factors of the local deformation and stress of a silicon chip mounted on area-arrayed metallic bumps. It was also confirmed experimentally that both the hound’s-tooth alignment between a TSV (Through Silicon Via) and a bump and control of mechanical properties of electroplated copper thin films used for the TSV and bump is indispensable in order to minimize the packaging-induced stress in the three-dimensionally mounted chips. This test chip is very effective for evaluating the packaging-process induced stress in 3D stacked chips quantitatively.

INTRODUCTION
So far, electronic products such as mobile phones and PCs have been miniaturized continuously and their functions have been improved drastically. Three dimensionally stacked structures such as multi-chip modules and multi-chip packages are indispensable for these products in order to increase the assembly density. System in package (SiP) and chip on chip (CoC) of the multi chip structures have been already used in actual products. In addition, the methods of the interconnection between an LSI chip and a substrate or another chip has been changed from a wire-bonding structure (WB) to a flip-chip structure (FC) for maximizing the interconnection density (1-3). The flip-chip technology using an area-arrayed solder bumps has been already employed in the three-dimensionally
stacked packages mentioned above. Since the total thickness of the stacked structure is strictly limited for mobile application, in particular, each chip has been thinned to less than 50 μm to minimize the total thickness of the modules or packages.

These flip-chip structures using area-arrayed tiny metallic bumps such as Cu or Au are surrounded by insulating material (underfill) such as epoxy or plastic for assuring the reliability of the connection between an LSI chip and a substrate or another chip. The authors have already reported that the local distribution of the residual deformation and residual stress on a transistor formation surface of a chip is changed drastically by changing the interconnection structure of packages or modules from a wire-bonding structure to an area-arrayed flip-chip bonding structure (4, 5). In particular, a periodic stress with amplitude of more than 100 MPa appears due to the periodic alignment of metallic bumps because of the mismatch in the material properties such as the coefficient of elasticity and the thermal expansion coefficient between metallic bumps and underfill material even in a SOS (Silicon On Silicon) structure. The periodic stress distribution was validated by measurement using stress sensing chips with poly-crystalline-silicon-film gauges of 10 μm in length (5). Such local deformation and stress deteriorate the mechanical reliability of the jointed structure.

In addition, the mechanical properties of electroplated copper bumps such as Young’s modulus and yield stress were found to vary drastically depending on their micro texture (6). The microstructure of the electroplated materials varies depending on their electroplating conditions and thermal hysteresis after the electroplating. Therefore, the final residual stress in the stacked chips is dominated by not only the stacked structure but also the process-dependent mechanical properties of the materials used for interconnection. Since the residual stress causing the shift of electronic performances of devices, it is very important to control it for assuring the reliability of products (7-9).

In this paper, the amplitude of the variation of the residual stress in the three-dimensionally stacked silicon chips was analyzed using a three-dimensional finite element method as functions of the cross-sectional structure of the interconnection between the stacked chips and material properties of area-arrayed fine bumps. Also, the estimated residual stress was validated by stress-sensing test chips in which 2-μm long piezoresistance strain gauges were embedded.

**FINITE ELEMENT ANALYSIS MODEL FOR INVESTIGATING THE RESIDUAL STRESS DISTRIBUTION IN STACKED LSI CHIPS**

Figure 1 shows an example of a three-dimensional finite element model for the stress analysis. Assuming the symmetry of the total structure, one fourth of the total structure was modeled for the structural analysis. Area arrayed bump alignment was assumed. The diameter and the height of Cu bumps were fixed at 200 μm and 50 μm, respectively and the pitch of the bump was varied from 5μm to 1000 μm. The width of the chip was assumed to 5 mm. A hexahedral solid mesh with 20-node was used for the analysis. The total numbers of nodes and elements were about 65,000 and 60,000, respectively. The chip was mounted on a silicon substrate with the electroplated tin/copper bumps at 150°C. The thickness of the chip was varied from 280 μm to 50 μm. The materials constants used in the stress analysis are summarized in Table 1. Most materials were assumed to be elastic. Only Cu bumps were modeled as elastic-plastic material. Though silicon is anisotropic material, it was assumed to be isotropic material with Young’s modulus of 167 GPa to simplify the analyses. This assumption may cause some error when the estimated results are compared with the experimental results.

In addition, it was found that the mechanical properties of electroplated copper varied drastically depending on its electroplating condition and thermal history after the electroplating as shown in Fig. 2. This figure summarizes the change of the stress-strain curve of electroplated copper thin films as a function of annealing temperature after electroplating. Not only Young’s modulus of the film but also the yield stress and fracture strain changed drastically with the increase of the annealing temperature. This is due to the change of the micro texture of the films.

In order to discuss the effect of the mechanical properties of underfill material on the local deformation and stress of the silicon chip mounted on the area-arrayed bumps, the test underfill materials were prepared by varying the content of filler from 0wt.% to 65wt.% . The material properties of the

---

**Fig. 1 Three-dimensional finite element model for analysis of residual stress in a Si chip mounted on the area-arrayed fine bumps**

**Table 1 Materials constant**

<table>
<thead>
<tr>
<th>Material</th>
<th>Young’s modulus (GPa)</th>
<th>Poisson’s ratio</th>
<th>Thermal expansion coefficient (10⁻⁶/K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>167</td>
<td>0.07</td>
<td>3.0</td>
</tr>
<tr>
<td>Cu bump</td>
<td>117</td>
<td>0.3</td>
<td></td>
</tr>
<tr>
<td>Substrate</td>
<td>167</td>
<td>0.07</td>
<td>3.0</td>
</tr>
<tr>
<td>Underfill</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(0 wt.%)</td>
<td>2.4</td>
<td>0.3</td>
<td>57</td>
</tr>
<tr>
<td>(40 wt.%)</td>
<td>5.1</td>
<td>0.3</td>
<td>39</td>
</tr>
<tr>
<td>(65 wt.%)</td>
<td>7.3</td>
<td>0.3</td>
<td>24</td>
</tr>
</tbody>
</table>

---

Copyright © 2011 by ASME
test underfill materials were measured by using a dynamic mechanical analysis method and a thermo mechanical analysis method as shown in Fig. 3. The measured results are also summarized in Table 1. These values were also applied to the analyses. To analyze the thermal residual stress in the stacked structures, thermal load from 175°C to 25°C was applied to each model.

**ESTIMATED CHANGE OF THE RESIDUAL STRESS IN A 3D STACKED CHIPS**

When the thickness of a Si chip is decreased to less than 200 μm, it has been found that the periodic stress distribution starts to appear even at a back surface of a Si chip depending on the pitch of the area-arrayed fine bumps. When the thickness of a Si chip was 50 μm, for example, the estimated maximum value of the principal stress reached about 150 MPa, and the amplitude of the periodic oscillation often exceeded 100 MPa (4, 5). Therefore, the decrease of the thickness of a Si chip causes serious increase of the residual stress even at a back surface of the Si chip, and the value of the stress may cause both electronic and mechanical failures of the Si chip. Since these local stress distributions were caused by the local deformation of the thinned silicon chip, it is also very important to evaluate the local deformation quantitatively in order to discuss the reliability of the stacked chips.

The local residual stress in a silicon chip also changes significantly depending on the alignment of the fine bumps and the material constant of underfill as shown in Fig. 4. Tensile stress appears in the chip on the underfill and compressive stress appears on the bump. This is caused by the local deflection of the silicon chip mounted on the area-arrayed bumps. The amplitude of the residual stress varied from about 60 MPa to 100 MPa depending on the bump pitch and the material constant of underfill. When the bump pitch was 400 μm, sinusoidal distributions of the residual stress appeared near the chip surface. The amplitude of the local stress increased from about 60 MPa to 80 MPa with the decrease of the filler content in the underfill. This means that the local residual stress increases with the increase of the coefficient of thermal expansion (CTE) of underfill.

The amplitude of the residual stress increased drastically when the bump pitch was widened from 400 μm to 600 μm. The effect of the CTE of underfill on the amplitude of the residual stress was enhanced when the bump pitch was increased. This is because that free shrinkage of the underfill material during cooling from its curing temperature to room temperature can occur around the center area between two bumps. When the bump pitch is decreased, the shrinkage of underfill is prohibited by the attached bump of which CTE is smaller than that of underfill. Thus, the amplitude of the local residual stress in a silicon chip is determined by not only the material constant of underfill but also the structural parameter of the flip chip structure, i.e., bump pitch.

Fig. 2 Change of the stress-strain curve of the electroplated copper thin films as a function of the annealing temperature

Fig. 3 Dynamic and thermo mechanical analyses of test underfill materials
Similarly, the effect of the Young’s modulus of the electroplated copper bumps under the mounted chip on the local residual stress on the chip surface was analyzed as shown in Fig. 5. As was expected, the estimated amplitude of the periodic stress distribution decreased from about 120 MPa to 65 MPa when the Young’s modulus of the bumps was decreased from 130 GPa to 20 GPa which was the minimum value of the measured result shown in Fig. 2.

Next, the effect of the relative position of a bump to a via in the interconnection on a silicon chip was analyzed as shown in Fig. 6. In the model 6(a), a bump was jointed to a thick via in the interconnection, while it was jointed to a thin interconnection as shown in Fig. 6(b). The estimated change of the residual stress in a silicon chip mounted on the bumps is summarized in Fig. 7. It was found that both the maximum principal stress and the amplitude of the periodic stress distribution between two bumps decreased drastically when the bumps were not jointed to thick vias directly. The maximum amplitude of the periodic stress decreased from 200 MPa to 40 MPa, and the maximum principal stress also decreased from -210 MPa to -150 MPa.
The strain gauges we have developed can measure three dimensional stress components separately based on the anisotropic piezoresistance effect of single-crystalline silicon. Therefore, not only the mechanical properties of materials used for the stacked structure but also the cross-sectional structure of the interconnection between bumps and the mounted chip are the important factors which determine the final residual stress in the mounted chip.

MEASUREMENT OF THE LOCAL RESIDUAL STRESS

The estimated results were validated by experiment. Test flip chip substrates were made by silicon chip on which the area-arrayed tin/copper bumps were electroplated as shown in Fig. 8. The width of a bump was fixed at 200 μm, and the bump pitch varied from 400 μm to 1000 μm. The thickness of the copper layer was about 40 μm and that of tin layer was about 10 μm. This tin layer was used for the rigid joint formation by alloying with copper interconnections formed on a stress sensing chip.

The local distribution of the residual stress was measured by using stress sensing chips in which the piezoresistive strain gauges were embedded as shown in Fig. 9. The length of each gauge was 2 μm, and an unit cell consisted of 4 gauges with different crystallographic directions as shown in Fig. 9. This alignment of strain gauges enables to measure the tensor component of three-dimensional stress fields separately (10).

The strain gauges we have developed can measure three dimensional stress components separately based on the anisotropic piezoresistance effect of single-crystalline silicon by aligning 4 gauges along different directions. When the direction of the gauges is rotated by 45 degrees with each other as shown in Fig. 6, the relation between the resistivity change and stress components can be expressed as is summarized in

\[
\begin{align*}
\frac{\Delta \rho_x}{\rho_0} &= \frac{1}{2} \left( \sigma_{xx} + \sigma_{yy} + \sigma_{zz} \right) + \frac{1}{2} \left( \sigma_{yy} + \sigma_{zz} + \sigma_{xx} \right),
\frac{\Delta \rho_y}{\rho_0} &= \frac{1}{2} \left( \sigma_{yy} + \sigma_{zz} + \sigma_{xx} \right),
\frac{\Delta \rho_z}{\rho_0} &= \frac{1}{2} \left( \sigma_{zz} + \sigma_{xx} + \sigma_{yy} \right),
\frac{\Delta \rho_{xy}}{\rho_0} &= \frac{1}{2} \left( \tau_{xy} + \tau_{yz} + \tau_{zx} \right),
\frac{\Delta \rho_{yz}}{\rho_0} &= \frac{1}{2} \left( \tau_{yz} + \tau_{zx} + \tau_{xy} \right),
\frac{\Delta \rho_{zx}}{\rho_0} &= \frac{1}{2} \left( \tau_{zx} + \tau_{xy} + \tau_{yz} \right).
\end{align*}
\]

(a) Bump pitch: 400 μm
(b) Bump pitch: 600 μm
(c) Bump pitch: 800 μm
(d) Bump pitch: 1000 μm

Fig. 8 Test substrate for measuring the local deformation and residual stress of a silicon chip

The estimated results were validated by experiment. Test substrates with area-arrayed bumps were electroplated as shown in Fig. 8. The width of a bump was fixed at 200 μm, and the bump pitch varied from 400 μm to 1000 μm. The thickness of the copper layer was about 40 μm and that of tin layer was about 10 μm. This tin layer was used for the rigid joint formation by alloying with copper interconnections formed on a stress sensing chip.

The local distribution of the residual stress was measured by using stress sensing chips in which the piezoresistive strain gauges were embedded as shown in Fig. 9. The length of each gauge was 2 μm, and an unit cell consisted of 4 gauges with different crystallographic directions as shown in Fig. 9. This alignment of strain gauges enables to measure the tensor component of three-dimensional stress fields separately (10).

The strain gauges we have developed can measure three dimensional stress components separately based on the anisotropic piezoresistance effect of single-crystalline silicon by aligning 4 gauges along different directions. When the direction of the gauges is rotated by 45 degrees with each other as shown in Fig. 6, the relation between the resistivity change and stress components can be expressed as is summarized in

\[
\begin{align*}
\frac{\Delta \rho_x}{\rho_0} &= \frac{1}{2} \left( \sigma_{xx} + \sigma_{yy} + \sigma_{zz} \right) + \frac{1}{2} \left( \sigma_{yy} + \sigma_{zz} + \sigma_{xx} \right),
\frac{\Delta \rho_y}{\rho_0} &= \frac{1}{2} \left( \sigma_{yy} + \sigma_{zz} + \sigma_{xx} \right),
\frac{\Delta \rho_z}{\rho_0} &= \frac{1}{2} \left( \sigma_{zz} + \sigma_{xx} + \sigma_{yy} \right),
\frac{\Delta \rho_{xy}}{\rho_0} &= \frac{1}{2} \left( \tau_{xy} + \tau_{yz} + \tau_{zx} \right),
\frac{\Delta \rho_{yz}}{\rho_0} &= \frac{1}{2} \left( \tau_{yz} + \tau_{zx} + \tau_{xy} \right),
\frac{\Delta \rho_{zx}}{\rho_0} &= \frac{1}{2} \left( \tau_{zx} + \tau_{xy} + \tau_{yz} \right).
\end{align*}
\]

(a) Stress-sensing chip
(b) Strain gauges formed on a (001) crystallographic plane of silicon

Fig. 9 Stress sensing chip with embedded strain gauges
respectively. These results agreed well with the estimated ones (11). Thus, the coefficient of thermal expansion of underfill is one of the dominant factors of the local deformation of a silicon chip. This local deformation can be seen clearly without a microscope as shown in Fig. 11.

Figure 12 summarizes the effects of bump pitch and mechanical properties of underfill on the local deformation of a silicon chip. The amplitude of the local deformation increased monotonically with the increase of the bump pitch. This is because that the underfill between two bumps could shrink easily (freely) when the bump pitch increased. In addition, the local deformation increased with the decrease of the filler content when the bump pitch was larger than 1 μm. Since the decrease of the filler content increases the CTE of underfill, the shrinkage of the underfill mainly dominated the amplitude of the local deformation. On the other hand, the local deformation increased with the increase of the filler content when the bump pitch was shorter than 0.8 μm. When the bump pitch becomes shorter, the free shrinkage of the underfill is strictly prohibited by metallic bumps. Thus, the underfill with higher Young’s modulus increased the local deformation in this structural area. This result indicates that the material selection of the underfill should be determined by considering the pitch of the area-arrayed bumps.

Figure 13 shows an example of the measured distribution of the residual stress between two bumps. Figure 13(a) shows the effect of underfill material on the amplitude of the residual stress. In this example, the bump pitch was fixed at 400 μm and the thickness of the sensor chip was 280 μm. The local periodic distribution clearly appeared between the bumps, and the amplitude of the residual stress distribution increased from about 80 MPa to about 100 MPa when the content of filler in the underfill decreased from 65 wt.% to 0 wt.%. This change
agreed well with the estimated results as was shown in Fig. 4(a).

The amplitude of the residual stress increased from about 90 MPa to 130 MPa when the bump pitch was changed from 400 μm to 600 μm, as shown in Fig. 13(b). The change mainly occurred in the area where the chip was on the underfill. The measured values also agreed well with the estimated ones shown in Figs. 4(a) and 4(b). This result clearly indicates that the shrinkage of the underfill and thus, the deformation of the silicon chip caused the local residual stress.

It was also confirmed that the Young’s modulus of underfill material plays an important role on the local deformation when the bump pitch was smaller than 600 μm and when the chip thickness was less than 100 μm. Thus, both the material constant of underfill and the alignment structure of fine bumps are the dominant factors of the local deformation and stress of a silicon chip mounted on area-arrayed metallic bumps.

CONCLUSION

The local distributions of the residual stress in the 3D chip-stacked structure were analyzed and measured by the piezoresistive strain sensors. The dominant structural factors of the local deformation and the residual stress of a silicon chip were investigated quantitatively based on the results of three-dimensional finite element analysis and measurements of the local deformation and residual stress of the chip mounted on area-arrayed metallic bumps. Not only the materials constants of underfill and metallic bumps such as the coefficient of thermal expansion and Young’s modulus but also the structural parameter such as the relative position between a bump and a via and bump pitch change the amplitude of the local deformation and the residual stress of a silicon chip mounted on the area-arrayed bumps drastically. The optimum mechanical properties of underfill, for example, are a strong function of the pitch of the area-arrayed bumps. It is, therefore, very important to optimize the combination of materials used for the stacked structure and the alignment structure of bumps and interconnections.

ACKNOWLEDGMENTS

This research work is partly supported by the Grants-in-Aid for Scientific Research and the Japanese special coordination funds for promoting science and technology. The authors would like to thank Prof. M. Koyanagi, and Prof. M. Esashi of Tohoku University for their helpful suggestions and discussions.

REFERENCES


