Evaluation of the Change of the Residual Stress in Nano-scale Transistors During the Deposition and Fine Patterning Processes of Thin Films

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Abstract
The embedded strain gauges in a PQC-TEG were applied to the measurement of the change of the residual stress in a transistor structure with a 50-nm wide gate during thin film processing. The change of the residual stress was successfully monitored through the process such as the deposition and etching of thin films. In addition, the fluctuation of the process such as the intrinsic stress of thin films and the height and the width of the etched structures was also detected by the statistical analysis of the measured data. The sensitivity of the measurement was 1 MPa and it was validated that the amplitude of the fluctuation exceeded 100 MPa. This technique is also effective for detecting the spatial distribution of the stress in a wafer and its fluctuation among wafers.

1. Introduction
Electronic products have been miniaturized continuously and their functions have been improved drastically. To keep the continuous improvement of the transistor performances, the structure of transistors should become complicated due to the applications of several technologies such as a FinFET structure, a SOI structure, and a strained Si structure with high-k dielectrics and metal gates. But, it is not easy to assure the functions and reliability of those complicated structures because not only the mismatch of the lattice constant between different materials, but also both a thermal and an intrinsic stresses that occur during thin-film processing vary the final residual stress in transistors drastically [1]. The residual stress causes the shift of electronic functions of dielectric and semiconductor materials and thus, gives rise to the unexpected shift of performance of transistors [2, 3] and the degradation of them due to the stress-induced diffusion of elements in the transistor structures [4]. In addition, such high stresses deteriorate the reliability of thin film interconnections by fatigue or creep damage of materials [5]. Therefore, it is important to control and optimize the residual stress in transistor structures. It is also important to elucidate the mechanism of the change of electronic performance of transistors which is caused by the concentration of stress at structure edges quantitatively. Since the residual stress is varied by the structure of the transistors such as width and inclined angle of a gate, there should be a distribution of the residual stress in a wafer depending on the allowance of the thin film processing. The residual stress also varies drastically as a function of the intrinsic stress in thin films which is a strong function of the film deposition conditions such as temperature of a wafer and substrate material on which the film is deposited. Therefore, it is not easy to estimate both the spatial and time-dependent distribution of the residual stress in a wafer quantitatively.

In this paper, the change of the residual stress in a transistor structure during the thin film processing such as the deposition and etching of thin films was investigated by applying the piezoresistive strain sensors embedded in a wafer before the thin film processing. In addition, the change of the residuals stress caused by the interference of the stress concentration fields between two gate-electrodes was measured by forming a periodic aligned gate structures on a sensor gauge. The measured data were compared with the estimated results which were analyzed by using a 3D finite element method considering the intrinsic stress of thin films used in the experiment. The fluctuation of the measured data in a wafer was attributed to the fluctuation of the finely patterned gate structure such as the width, thickness and the inclination of the patterned gate structures. Thus, the proposed method was found to be effective for evaluation the average residual stress in a transistor structure after the thin film processing and the distribution of the residual stress in a wafer quantitatively.

2. Embedded strain gauges and stress measurement
2-μm long strain gauges which consisted of n-type diffused resistors were embedded in a (001) silicon wafer as shown in Fig. 1. Piezoresistance effect is a change of resistivity by stress) of semiconductors such as silicon has been studied for measuring stress in a silicon chip. [7 - 10] The authors have adopted the piezoresistance effect of single-crystalline silicon to measure the residual stress in transistors because of following reasons. 1) Stress condition of semiconductors does not change by the installation of sensors. 2) The sensor can measure three dimensional stress components separately. 3) The sensor can measure the residual stress on a transistor formation surface of the stacked structure. 4) The size of the sensor can be miniaturized by semiconductor fabrication.
A relationship between the resistivity change and the three-dimensional stress components can be expressed by a tensor equation (1).

\[
\frac{\delta \rho}{\rho} = \begin{pmatrix}
\pi_{11} & \pi_{12} & \pi_{13} & \pi_{14} & \pi_{15} & \pi_{16} \\
\pi_{21} & \pi_{22} & \pi_{23} & \pi_{24} & \pi_{25} & \pi_{26} \\
\pi_{31} & \pi_{32} & \pi_{33} & \pi_{34} & \pi_{35} & \pi_{36} \\
\pi_{41} & \pi_{42} & \pi_{43} & \pi_{44} & \pi_{45} & \pi_{46} \\
\pi_{51} & \pi_{52} & \pi_{53} & \pi_{54} & \pi_{55} & \pi_{56} \\
\pi_{61} & \pi_{62} & \pi_{63} & \pi_{64} & \pi_{65} & \pi_{66}
\end{pmatrix}
\frac{\sigma}{\sigma}
\]

Where, \(\delta \rho / \rho\) is the resistivity change along i axis, when an electric current passed through j-axis. \(\sigma_{ii}\) is normal stress along each direction. \(\tau_{ij}\) is shear stress on ij plane. Piezoresistance coefficients \(\pi_{ij}\) (expressed in MPa\(^{-1}\)) are defined as components of a six by six matrix. For the cubic crystal structure such as silicon, the coefficients of matrix are reduce to three independent components: \(\pi_{11}, \pi_{12}\) and \(\pi_{44}\) due to the symmetry of crystallographic structure. This sensor can measure three dimensional stress components separately based on the anisotropic piezoresistance effect of single-crystalline silicon. [10, 11] When sensors gauges are aligned as shown in figure 4, the relation between resistivity change and stresses can be expressed as following equations.

\[
\frac{\delta \rho_{1}}{\rho_{1}} = \frac{1}{2} [\sigma_{11} + \sigma_{12} + \sigma_{14}] \varepsilon_{1} + \frac{1}{2} [\sigma_{11} + \sigma_{12} - \sigma_{14}] \varepsilon_{2} + \sigma_{15} \varepsilon_{3} \\
\frac{\delta \rho_{2}}{\rho_{2}} = \frac{1}{2} [\sigma_{11} + \sigma_{12} - \sigma_{14}] \varepsilon_{1} + [\sigma_{15} + \sigma_{16}] \varepsilon_{2} + \frac{1}{2} [\sigma_{11} - \sigma_{12}] \varepsilon_{3} \\
\frac{\delta \rho_{3}}{\rho_{3}} = \frac{1}{2} [\sigma_{11} + \sigma_{12} + \sigma_{14}] \varepsilon_{1} + \frac{1}{2} [\sigma_{15} + \sigma_{16}] \varepsilon_{2} + \sigma_{15} \varepsilon_{3} \\
\frac{\delta \rho_{4}}{\rho_{4}} = \frac{1}{2} [\sigma_{11} + \sigma_{12} - \sigma_{14}] \varepsilon_{1} + \frac{1}{2} [\sigma_{15} + \sigma_{16}] \varepsilon_{2} + \sigma_{15} \varepsilon_{3} \\
\frac{\delta \rho_{5}}{\rho_{5}} = \frac{1}{2} [\sigma_{11} + \sigma_{12} + \sigma_{14}] \varepsilon_{1} + \frac{1}{2} [\sigma_{15} + \sigma_{16}] \varepsilon_{2} + \sigma_{15} \varepsilon_{3} \\
\frac{\delta \rho_{6}}{\rho_{6}} = \frac{1}{2} [\sigma_{11} + \sigma_{12} - \sigma_{14}] \varepsilon_{1} + \frac{1}{2} [\sigma_{15} + \sigma_{16}] \varepsilon_{2} + \sigma_{15} \varepsilon_{3}
\]

This sensor chip was made in the NMC (Nano-Machining Center, Tohoku University). 1420 gauges were formed on a 8 mm x 8 mm silicon chip. When the normal stress perpendicular to the wafer surface is negligibly small, in-plane stress components can be determined separately by measuring the change of the resistance of the 4 gauges shown in this figure. The typical value of the piezoresistance coefficient (\(\pi_{11} + \pi_{12}\)) of the gauges was about -5.2 x 10\(^{-4}\)/MPa. These gauges were embedded in a PQC-TEG for discussing the change of the local distribution of the residual stress during thin-film processing. In this study, the changes and their fluctuation of the residual stress in a 45-nm wide transistor structure were measured. The intrinsic stress of sputtered films was varied from -4 GPa to +2.5 GPa by changing the film deposition conditions such as substrate temperatures and ambient gas pressure.

The change of the residual stress in a sensor formation area caused by this tungsten film deposition was analyzed by a finite element analysis. Fig. 2 shows the FEM-analysis model. The substrate is silicon and sufficiently large comparing to the strain gauges. The residual compressive stress of 4 GPa in the tungsten thin film and 400 MPa in the silicon dioxide film were taken into account in this analysis. The total number of the nodes and elements are 48734 and 43990, respectively. The three-dimensional plain strain model is applied to this analysis. The materials constants used in this analysis are summarized in Table 1. All materials were assumed to be elastic material.

Table 1: Materials constant

<table>
<thead>
<tr>
<th>Material</th>
<th>Young's Modulus (GPa)</th>
<th>Poisson ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>170</td>
<td>0.07</td>
</tr>
<tr>
<td>Silicon oxide</td>
<td>70</td>
<td>0.17</td>
</tr>
<tr>
<td>Tungsten</td>
<td>408</td>
<td>0.17</td>
</tr>
</tbody>
</table>

Figure 3(a) shows schematic cross-section of a silicon chip with sensor gauges. The stress analysis was performed by FEM considering this simple structure showed in Fig. 3(b). Figure 4 shows the color contour of the stress field in the structure after the slit formation in the tungsten thin film. It was found that the effect of
residual stress of the sputtered tungsten thin film reaches the area of sensor gauges. The change of the average value of the residual stress in the area of sensor gauge by the sputtered tungsten thin film was about 25 MPa. Then, it was also found that the effect of stress concentration fields at the edges of the slit reaches the area of strain gauges. The averaged change of the residual stress in a transistor by forming the slit was about 70 MPa.

3. Evaluation of the change of the residual stress during thin film processing

The change of the residual stress in a substrate during a simple fabrication process of periodically aligned transistor gate with side spacers was measured using the strain gauges as shown in Fig. 5.

First, 50-nm thick tungsten film was deposited on the strain gauges and a slit was formed around the center area of the deposited film as was shown in Fig. 4. The intrinsic stress of sputtered tungsten film was varied from -4 GPa to +2.5 GPa by changing the deposition conditions such as substrate temperatures and ambient gas pressure.

It was possible, therefore, to discuss the effects of the intrinsic stress in thin films and the pitch of the patterned structures on the final residual stress in the substrate under the patterned film separately by changing the deposition condition of the tungsten film. The width of the patterned tungsten film was varied from 1 μm to 20 nm. The change of the resistance of each gauge caused by the thin film processing was measured after each process.

Figure 6 shows an example of the change of the residual stress in a strain gauge caused by the film deposition and 1-slit formation at the center of the gauge. In this example, the intrinsic stress of the tungsten film was about -4 GPa. When the film was deposited on the gauge, the tensile stress of about 20 MPa appeared in the gauge. On the other hand, the average residual stress changed to compressive stress of about 35 MPa after 1-μm wide slit formation. Since there was high compressive stress in the deposited film, the expansion of the film caused the compressive stress in the area where the film was etched off as shown in Fig. 7. The compressive stress decreased when the width of the slit was decreased. In addition, it returned to tensile stress when the slit width was less than 100 nm. These changes were validated by finite element analyses.

Then, the change of the residual stress was measured after the formation of periodically aligned slits as shown in Fig. 8. In this study, the width of the slit and the space between the slits (L&S) was fixed at same value. Fig. 8(a) shows the SEM (Scanning Electron Microscopy) image of the periodically aligned 200-nm wide slits and Fig. 8(b) is
that of 100-nm wide slits. These slits were formed on each 2-μm long strain gauge. The width of the slit was varied from 20 nm to 1 μm.

When the periodically aligned slits were formed in the tungsten film, the compressive stress increased monotonically when slits were formed periodically as shown in Fig. 8. The compressive stress increased from about 35 MPa to 110 MPa when the number of slits formed on the 2-μm long gauge was increased. When the number of the slit increased, the pitch of the patterned film decreased linearly. Since the decrease of the pitch should enhance the interference of the nearby stress concentration fields which was generated at each patterned edge, this increase of the residual stress in finely patterned structures can be explained by the interference of the stress concentration fields. These results were also validated by finite element analyses quantitatively.

These results indicate that the final residual stress in a substrate is functions of not only the intrinsic stress in the film deposited on the substrate and the finely patterned structure. In this study the measured maximum difference in the residual stress in a substrate was about 130 MPa when a width of a slit was 20 nm. Since the stress sensitivity of the transconductance of NMOS is about 0.2%/MPa, the performance of transistors in a wafer may vary by about 26%, even when the intrinsic stress in the deposited film is uniform in a wafer. Therefore, it is very important to monitor the residual stress in transistors during manufacturing to assure both the performance and reliability of products.

Next, the effect of the deposition of a thin side spacer film was investigated as shown in Fig. 5. A 50-nm thick silicon dioxide film was deposited on the strain gauge and the plural slits were formed periodically by using a focused ion beam. Then, a 20-nm thick tungsten film was deposited on the slit structures. Figure 9 shows an example of the change of the residual stress during the fabrication process of a transistor. The minimum width of a gate was 45 nm. In this example, the intrinsic stress of the gate film was about -4 GPa, and that of the side spacer film was about -1.6 GPa. The thickness of the side spacer film was about 5 nm. The averaged stress in the structure changed from the initial value of about 30 MPa which was caused by the deposition of the gate film to the second value of about – 20 MPa which was caused by patterning, and finally to the third value of about -8 MPa after the deposition of the side spacer film. Thus, the change of the residual stress during the transistor formation process was successfully monitored by this method. Even though the thickness of the side spacer film was thinner than the width of the gate, the change rate of the residual stress was rather large. This was due to the sharp stress concentration at each gate edge and the interference of the stress concentration fields.

The measured results were compared with the analyzed results as shown in Fig. 10. Figure 10(a) is the comparison of the measured result of the periodically aligned 100-nm wide gate structures. The initial tensile stress of about 30 MPa changed to compressive stress of about 20 MPa due to the periodical L&S structure as was indicated in Fig. 8. The compressive stress was reduced by the deposition of the 20-nm thick side spacer by about 15 MPa. Similarly, the residual stress in the periodically aligned 200-nm wide gate structures changed from the initial tensile stress to compressive stress of about 30 MPa, and shifted to about tensile stress of about 10 MPa. These changes agreed well with the analyzed results, respectively. However, the change rate in the 100-nm wide gate was smaller than that of the 200-nm wide gate, though there should have been higher interference of the nearby stress concentration fields as shown in Fig. 8. The reason for this contradiction was found that the depth of the slits in the 200-nm wide gate structures was larger.
than that in the 100-nm wide gate structures. Considering the difference of the depth of each slit, it was confirmed that the measured results agreed well with the analyzed results.

In addition to the fluctuation of the depth of the slits, a wide distribution of the measured change of the residual stress was observed in some wafers as shown in Fig. 11. This figure shows an example of the wide distribution of the measured change of the residual stress after the periodic slit formation in a wafer. The average stress was shown in Fig. 10. It is clearly seen that the amplitude of the distribution in the 100-nm wide gate structure is larger than that in the 200-nm wide gate structure in this example. Since the fluctuation of the sensitivity of the developed strain gauges was within 20%, this wide discrepancy could not be explained by the fluctuation of the sensor sensitivity.

Thus, the fluctuation of the patterned gate structures was observed precisely by SEM. Figure 12 shows the typical examples of the observed fluctuation of the cross-sectional structures of the patterned gate structures. It is clearly seen that the patterned structures showed wide variation of both the width and the inclination angle of the side wall. The measured deviations of the width of the slits among about 100 samples were 100 nm +/- 23 nm and 200 nm +/- 21 nm, respectively. Thus, it was concluded that these deviations of the patterned gate structures was the main reason for the wide distribution of the change of the residuals stress under the patterned structures. Since the relative deviation of the 100-nm wide gate structure was about twice larger than that of the 200-nm wide gate structures, the amplitude of the distribution of the change of the residual stress under the 100-nm wide gate structures was higher than that under the 200-nm wide gate structure.

These results clearly indicate that the final residual stress in a transistor structure varies drastically depending on not only the intrinsic stress in the deposited thin films but also the patterned structure of the deposited film. Since there are various structures of transistors in a silicon chip, it is very difficult to keep the residual stress among plural transistors uniform. In addition, it is well-known that there is a distribution of the intrinsic stress in thin films in a wafer and among wafers. Thus, it is also difficult to control the residual stress in mass production. Since the relative deviation of the patterned fine structures should increase with the decrease of the minimum size of a transistor, the minimization of the fluctuation of the electronic performance of transistors should become one of the seriou issues to be solved in mass production. Therefore, this monitoring method of the residual stress in a transistor structure should be an effective tool for controlling the residual stress during thin-film processing, and for detecting the critical process which dominates the failure caused by the residual stress.
4. Conclusions
The change of the residual stress in a transistor structure during thin-film processing was successfully monitored in-situ by applying embedded strain gauges in a wafer. Piezoresistance effect of single-crystalline silicon was applied to the strain gauges. Four strain gauges with different crystallographic direction were embedded on a (001) silicon wafer to detect the two-dimensional stress components separately. The change of the residual stress in the silicon wafer was measured by depositing thin films on the gauges. Some slits were formed by a focused ion beam in the deposited films. The width of the slits was varied from 1 μm to 20 nm. It was found that the residual stress changed from the initial tensile stress of about 30 MPa to the compressive stress of about 30 MPa when a 50-nm thick tungsten film with the intrinsic stress of about -4 GPa was deposited on the gauges. The compressive stress decreased with the decrease of the width of a slit formed on the center of the gauges. On the other hand, the compressive stress increased monotonically with the decrease of the width of the periodically aligned slits. This was due to the interference of the nearby stress concentration fields which appeared at the edges of the patterned gate. It was also confirmed that the final residual stress in a transistor is varied by the fluctuation of both the intrinsic stress in the deposited thin films and the cross-sectional structure of the patterned film. Therefore, it is very important to monitor the stress for assuring the reliability of the thin-film processing. Thus, this embedded strain-gauge technique is very effective for monitoring the fluctuation of the residual stress in a transistor in mass production.

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References